Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY

DEPARTMENT OF INFORMATION SCIENCE AND ENGINEERING

The Enclosed documents are verified and approved

HOD,ISE

HEAD
Dept. of Information Science & Engg.
Dr. Ambedkar Institute of Technology
Bangalore-560 056.

SEMESTER LESSON PLAN (Theory)

Department of ISE

UG Autonomous – BE in Information Science & Engineering

(THEORY SUB – 1)

LESSON PLAN for academic year 2021 - 22 ; (Odd Sem : October 2021 to JAN 2022)

Class / Sem / Sec	:	III Semester
Subject Name	:	**DIGITAL PRINCIPLES AND LOGIC DESIGN**
Subject Code :		18IS34
Start of semester (Commencement)	:	18-10-2021
End of semester (Last working day)	:	19-02-2022
Ref. Doc. No. Issue No. & Date	:	

As per syllabi (periods reqd.)	39	Actual classes reqd. (periods)	39	Sp. classes reqd. (periods)	-	No. of units in syllabi	5

Total number of periods required (for completing the syllabus) as per Lesson Plan	:	
Total number of periods available (for completing the syllabus) as per Time-Table & calendar of events (COE)	:	

No. of hrs. / periods prescribed by university (for completing the syllabus)	:	03	
No. of credits prescribed by the university (for completing the syllabus)	:	3:0:0	
Excess periods taken apart from planned periods / hours	:		
No. of hrs. / periods actually taken for the whole semester at the end	:		
Have you prepared the notes of the theory subject as per lesson plan?	:	Yes	No
If portions completed early before the planned periods (write the no. of classes taken), what is the reason for finishing early ? Even in the planned periods or even after taking extra classes, if syllabus is not completed (all the units/modules), what is the reason?	:		

Test / Exam dates scheduled & conducted as per Calendar of Events (COE)		**Planned**	**Conducted**
CIE Test – I	:	6 to 8th Dec 2021	8-12-2021
CIE Test – II	:	10 to 13th Jan 2021	15-2-2022
CIE Test – III	:	Jan 31 to Feb 3 2021	23-3-2022
Theory exam date (SEE) - Final	:	7-March to 25 March 2022.	

Unit	Ln No.	Lesson / Topics to be planned-covered as per the teaching plan	Planned Date	Actual Date	Sign	Re
I	L 1.	Definitions for Digital Signals, Digital Waveforms, Digital Logic.	22/10/21	22/10		
	L 2.	**Digital Logic:** Overview of basic gates and universal gates, AND-OR-Invert Gates, Positive and Negative Logic	22/10/21	22/10		
	L 3.	Combinational Logic Circuits: Boolean Laws and Theorems	23/10/21	23/10		
	L 4.	Sum-of-Products Method, Truth Table to Kamaugh Map, Pairs, Quads, and Octets	25/10/21	25/10		
	L 5.	Karnaugh Simplifications for 4 variables	29/10/21	29/10		
	L 6.	Don't-care Conditions	30/10/21	30/10		
	L 7.	Product-of-Sum,Product-of-sums Simplification	30/11/21	6/11		
	L 8.	Simplification using Quine McClusky Method.	6/11/21	8/11		
II	L 9.	Data-Processing Circuits: Multiplexers	8/11/21	12/11		
	L 10.	Multiplexers	12/11/21	12/11		
	L 11.	Demultiplexers	12/11/21	13/11		
	L 12.	1-of-16 Decoder	13/11/21	15/11		
	L 13.	Encoders	15/11/21	19/11		
	L 14.	Encoders	20/11/21	19/11		
	L 15.	Magnitude Comparator	19/11/21	20/11		
	L 16.	HDL Implementation of Data Processing Circuits	20/11/21	26/11		
III	L 17.	Flip-Flops: Flip-flops: RS FLIP-FLOPs , Gated FLIP-FLOPs Edge-triggered RS FLIP-FLOPs,	26/11/21	26/11		
	L 18.	Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs, , Various: A Synthesis Example, HDL Implementation of Flip-flops	26/11/21	26/11		
	L 19.	JK Master-slave FLIP-FLOPs	10/12/21	27/11		
	L 20.	Representations of FLIP-FLOPs	10/12	27/11		
	L 21.	Conversion of FLIP-FLOPs	11/12	29/11		
	L 22.	Types of Registers,	20/12	29/11		
	L 23.	Applications of Shift Registers,	24/12	11/12		

	L 24.	Register Implementation using HDL	24/12	13/12		
IV	L 25.	**Counters:** Introduction	27/12	13/12		
	L 26.	Asynchronous Counters	31/12	16/12		
	L 27.	Asynchronous Counters	31/12	17/12		
	L 28.	Synchronous Counters	3/1	17/12		
	L 29.	Synchronous Counters	7/1	18/12		
	L 30.	Decade Counters	7/1	20/12		
	L 31.	Counter Design as a Synthesis problem	8/1	23/12		
	L 32.	Counter Design using HDL	15/1	27/12		
V	L 33.	Design of Synchronous Sequential Circuit:	17/1	1/1/22		
	L 34.	Model Selection	21/1	1/1/22		
	L 35.	State Transition Diagram,	21/1	3/1/22		
	L 36.	State Synthesis Table	22/1	7/1/22		
	L 37.	Design Equations and Circuit Diagram	24/1	7/1/22		
	L 38.	State Reduction Technique-1	28/1	8/1/22		
	L 39.	State Reduction Technique-2	28/1	10/1/22		

Percentage of portions covered (No. of units covered / total no. of units)	100 %
Reason for not completing 100 % syllabus	

Text-books (T) / Reference-books (R) - University Prescribed / Referred (Author, Title of Book, Edition, Publisher, Year) to be mentioned in order

Text Books Followed :	Donald P Leach, Albert Paul Malvino & Goutam Saha: Digi Principles and Applications, 7th Edition, Tata McGraw Hill, 2011
Reference Books followed :	1.Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2nd Edition, Tata McGraw Hill, 2005. 2.Charles H. Roth: Fundamentals of Logic Design, Jr., 5th Edition, Thomson, 2004. 3.Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss: Digital System Principles and Applications, 10th Edition, Pearson Education, 2007. 4.R D Sudhaker Samuel, K.S. Nandini Prasad: Logic Design, 1st editi Elsevier Publication, 2013.
Websites : Any other sources	www.nptel.ac.in

	Nos.	Dates with details
No. of assignments given with date	3.	10-12-21, 24-12-21,
No. of question banks given with date		
No. of tutorial classes conducted with dates		
No. of remedial classes conducted with dates		
No. of weak students classes cond. with dates		
No. of counseling/s done as mentor		
No. of teaching methodologies & aids used		
Lesson planning done for theory & lab	✓	
Notes prepared for the subjects handled	✓	
Work dairy completed		
No. of memos / warnings / notices given	—	

Faculty's Name & Sign | **Reviewed by Name & Sign** | **HOD Name & Sign** | **Dean Name & Sign** | **Principal Name & Sig**